RESEARCH FINAL REPORT INTERNATIONAL COLLABORATION AND SCIENTIFIC PUBLICATION

FIRST YEAR

TO DESIGN THE ANALOG TO DIGITAL CONVERTER (ADC) BY USING ASYNCHRONOUS METHOD AIMS AT PRODUCING ADC CHIP FOR VIDEO SIGNAL CONVERSION APPLICATION

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RATIFICATION OF FINAL REPORT

Research Title : TO DESIGN THE ANALOG TO DIGITAL CONVERTER (ADC) BY USING ASYNCHRONOUS METHOD AIMS AT PRODUCING ADC CHIP FOR VIDEO SIGNAL CONVERSION APPLICATION

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2. Funding and Research Duration

a. Research Duration in Proposing : 3 years
b. The Total Budget proposed : Rp. 559.250.000,-
c. Fist year Budget Approved : Rp. 173.000.000,-

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Depok, 26 November 2012
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Executive Summary

Asynchronous ADC design with N comparator method is successfully finished. This ADC is used for embedded systems that have specifications: low power consumption, high speed, high resolution, and small size. This research is to improve the performance of pipeline that has been designed by applying asynchronous clock system with the same hardware structure. To realize the design of asynchronous ADC, step is do the design and simulation using Mentor Graphics software with AMS 0.35 µm technology CMOS process.

First step, studied ADC architecture to understand the characteristics of ADC. The results of the study to the understanding by exploring the key features of each type of topological A-ADC by comparing known characteristics that is most suitable for the design of the A-ADC's. Second step, designed a circuit forming units such as Asynchronous ADC comparator unit, switch capacitor units, digital logic units, and the units of SHA. Comparator circuit as a center for converting analog signals to digital signals, switch capacitor circuit is used as a feedback signal results as well as a provider of digital reference voltage for the comparator. Digital logic circuit functions as a digital signal processing, and circuit SHA function to analog signal sampling conversion. After designed digital logic and SHA circuits, then simulation is done. Third step, merge and simulating the circuit using eight comparator circuit eight, eight switch capacitor circuits, eight digital logic circuits and a series of SHA that forming an Asynchronous 8-bit ADC.

The results of the study with a frequency of 100 MHz, the voltage set point comparator showed 1.6 V, 0.012 µV offset voltage, 2.4 ns delay time. In linear output capacitor switch, the digital logic output steady at 3.3 V and the voltage shift sampling SHA maximum of 4 mV. Asynchronous 8-bits ADC require 576 MOS transistors and 9 capacitors and power 10.62 mW.

PREFACE

First , I would like to thank my GOD who has given a good healthy , ease in performing this research, thus successfully created a report that describes the results of the design and simulation of high speed asynchronous ADC.

The present and future design of System on Chip (SOC) will always evolve and is required for the development of the electronics industry applicability is widely used in the world of information technology.

It is a matter of pride, especially for a team of researchers successfully designed Asynchronous ADC (A-ADC), which is the latest development in the design of ADC. Besides, with an international publication has been submitted to international journal (Hindawi VLSl) and accepted in an international conference of the ICNMED, Hongkong, 19-20 Dec., will have an impact for the improvement and recognition of the publication by readers and researchers abroad so that little by little will increase Indonesia international publications and at least match even overtaking of international publications Malaysia.

Hopefully these results can boast of an institution where the research team shelter, Higher Education, as a partner institution overseas research and Indonesian communities.

This research could be finished as it is supported by many parties. Therefore, we take this opportunity to say a glad thank you to:

1. Higher Education gives the opportunity to conduct research with financing provided to the researcher team.
2. Rector of Gunadarma University who always supported and facilitated the ease to the researcher team.
3. Prof. Dr. Michel Paindavoine from LEAD Laboratory of Burgundy University France that helped in terms of solution, facility for research internship and co-operation in the fabrication of A-ADC to come.
4. Staff and students, who have helped in the research processes, may get a blessing from God.

We are aware that our report is far from perfect and there is no ivory that is not cracked, the constructive criticism and suggestions are welcome.

Jakarta, 26 November 2012

Prof. Dr. Busono Soerowirdjo
Head Reseacher

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LIST OF FIGURE